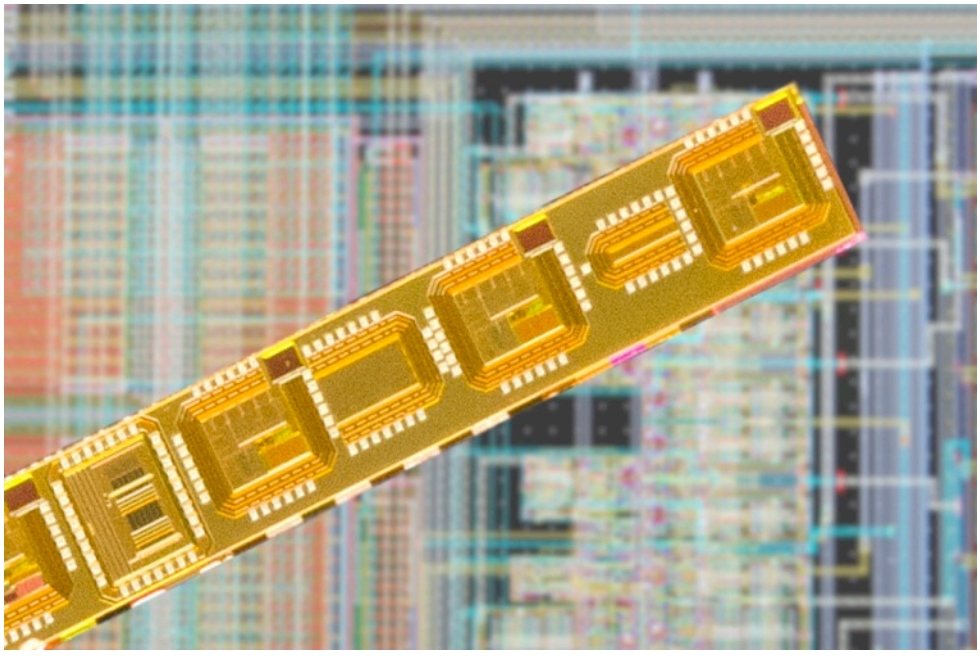
FRAUNHOFER INSTITUTE FOR INTEGRATED CIRCUITS IIS

PRESS RELEASE

First-Time-Right Design with Much Shorter Development Cycles

Erlangen/Dresden, April 20, 2015: The »Intelligent IP Mixed Signal Design Flow« methodology developed by the Design Automation group at the Fraunhofer Institute for Integrated Circuits IIS offers an unparalleled degree of automation, especially for the otherwise time-consuming, error-prone analog part of the design.



Intelligent IP mixed signal design: SMART sensor ASICs. © Fraunhofer IIS/EAS/ Sandra Kundel | Picture in color and print quality: www.iis.fraunhofer.de/en/pr

Integrated circuits that include both digital and analog elements, so-called mixed-signal ICs, are found in overwhelming numbers of today's microelectronic products, from consumer goods and critical automobile applications, to medical and aerospace sys-

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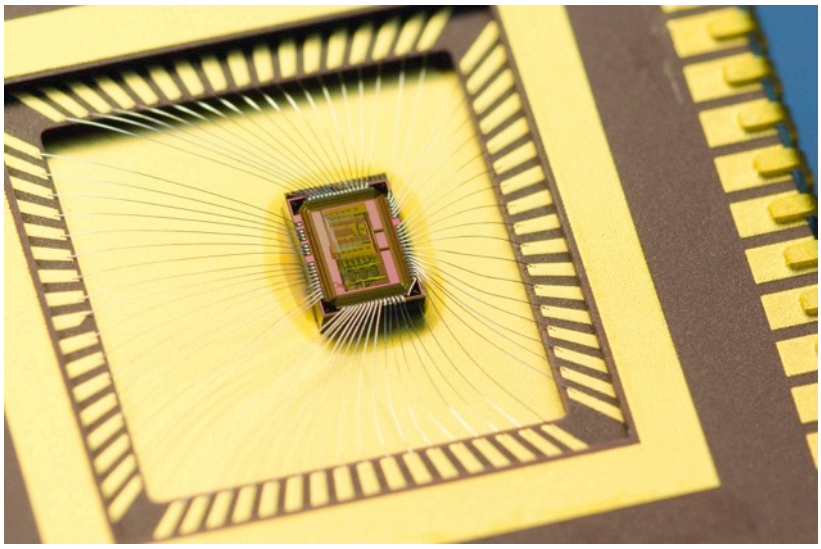
tems. Although the analog circuitry usually accounts for no more than 20 percent of the chip surface, the low degree of automation leads to high development costs and risky designs, a problem that is exacerbated by the growing reliance on miniaturization in semiconductor technologies.
The »Intelligent IP Mixed Signal Design Flow« methodology developed by the Design Automation group at the Fraunhofer Institute for Integrated Circuits IIS now offers an unparalleled degree of automation, especially for the otherwise time-consuming, error-prone analog portion of the design.

Integrated circuit design: low-cost, fast and reliable

In several development projects, design engineers at Fraunhofer IIS were able to demonstrate significant improvements in efficiency by using intelligent IP mixed signal design flows. During the design of a multiphysical SMART sensor ASIC for instance, they reduced development costs and time by 40 percent. The result was the creation of various ASICs for different requirements in a single development cycle. In future, efficiency gains will be realized even further through the automatic selection of the architecture during the system design. This innovative design flow was successfully used during the development of an industrial high-resolution A/D converter and an extremely fast image sensor. Johann Hauer, head of mixed signal ASIC development at IIS, has nothing but praise for the new methodology: »Although we have been striving for automated analog design processes for years, this complete design flow finally delivers the expected benefits for our daily development activities. A 40 percent reduction in development time and extremely reliable designs mean that we can finally offer first-time-right designs with much shorter development cycles. Another key factor is the very high acceptance level among our design engineers due to the intuitive approach.« Customers who outsource the development of mixed signal ASICs and IPs to Fraunhofer IIS can reap the benefits of this new design flow today. Customers who develop their own integrated circuits can adopt the new design flow beginning in 2016.

One development cycle for multiple applications and different technologies

The design flow currently supports established production technologies from various manufacturers, from 350 nm to 28 nm. Even now, researchers are driving the further development of future ultra-low-power 28 nm technologies in several research projects with the aim of demonstrating their utility in microelectronic systems used in safety-critical automobile applications and aerospace cabin communications.



ASIC with a high-resolution A/D converter (12-bit 20MSps ADC).
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Founded in 1985, **Fraunhofer Institute for Integrated Circuits IIS** in Erlangen, Germany, ranks first among the Fraunhofer Institutes concerning headcount and revenues. As the main inventor of mp3 and universally credited with the co-development of AAC audio coding standard, Fraunhofer IIS has reached worldwide recognition. In close cooperation with partners and clients the Institute provides research and development services in the following areas: Audio & Multimedia, Communications Systems, Energy Management, IC Design and Design Automation, Imaging System, Medical Technology, Non-destructive Testing, Positioning, Safety and Security Technology, Sensor Systems plus Supply Chain Management.

More than 830 employees conduct contract research for industry, the service sector and public authorities. Fraunhofer IIS with its headquarters in Erlangen, Germany, has further branches in Dresden, Fuerth, Nuremberg, Coburg, Deggendorf, Ilmenau, Wuerzburg, Bamberg and Waischenfeld. The budget of 108 million euros is mainly financed by projects. Less than 25 percent of the budget is subsidized by federal and state funds.

Detailed information on www.iis.fraunhofer.de/en.